REMARKS

Claims 12-18 have been canceled. Claims 1, 4, 5, 7 and 10-11 have been amended. Claims 1-11 remain for further consideration. No new matter has been added.

The rejections shall be taken up in the order presented in the Official Action.

1. The undersigned hereby authorizes an Examiner's amendment to change "multiplicant" to "multiplicand" in the specification. If the Examiner would rather have a replacement specification with this amendment, please contact the undersigned attorney and a replacement specification with this amendment shall be promptly provided.

2-3. Claims 12-18 currently stand rejected under 35 U.S.C. §112, second paragraph for allegedly failing to particularly point out and distinctly claim the subject matter deemed to be the present invention.

Claims 12-18 have been canceled.

4-5. Claims 1-18 currently stand rejected for allegedly being anticipated by the subject matter disclosed in U.S. Patent 4,031,377 to Deutsch (hereinafter "Deutsch").

Claims 1 and 7 recite a computing device on a *monolithic integrated* circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value. The Official Action contends that Deutsch discloses *"a computing unit on a monolithic integrated circuit..."*. (Official Action, pg. 3). However, it is respectfully submitted that a fair and proper reading of Deutsch fails to reveal that the device is located on a monolithic integrated circuit. Deutsch appears to be a combination of discrete components that are not all located on a monolithic integrated

circuit. In addition, the system of Deutsch is not a clocked system, which tends to further indicate that the system is not located on a monolithic integrated circuit.

In addition, the system of claim 1 recites *"means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicand;"*. (emphasis added, cl. 1). In contrast, the circuit disclosed in Deutsch generated a signal in product by utilizing right or left shift circuit 29 (FIG. 1). Deutsch makes this point emphatically clear when he states *"[t]he output of the shift circuit 29 is the multiplication product X=SC."*. (col. 5, lines 24-26). Hence, Deutsch clearly fails to disclose *"means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicand;"*.

A §102 rejection requires that a single reference teach each and every element of the claimed invention. Deutsch fails to disclose that the circuit is located on a monolithic integrated circuit. In addition, Deutsch also fails to disclose *"means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicand;"*. Therefore, it is respectfully submitted that Deutsch is incapable of anticipating claims 1 and 7.

6-7. Claims 5 and 11 currently stand rejected under 35 U.S.C. §103 in view of the combined subject matter disclosed in Deutsch in view of U.S. Patent 5,402,369 to Main (hereinafter "Main").

It is respectfully submitted that this rejection is now moot, since claims 1 and 7 are patentable for at least all the reasons set forth above.

For all the foregoing reasons, reconsideration and allowance of claims 1-11 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,

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